Refine Search

Search Results -

Terms	Documents
L1 same (signal near5 pin)	64

Database:
US Pre-Grant Publication Full-Text Database
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Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	L1 same (signal near5 pin)	64	L3
L2	L1 and (signal near5 pin)	155	L2
L1	(select$4 near3 path) near10 pin	502	L1

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Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	L1 same (signal near5 pin)	64	L3
L2	L1 and (signal near5 pin)	155	L2
L1	(select$4 near3 path) near10 pin	502	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
(439/189 |439/497 |439/507 |439/620 |439/505 |174/34 |361/683 |361/686 |361/752 |361/760 |709/253 |710/3 |710/100 |710/300 |710/305 |710/301 |710/316 |710/1 |710/313 |710/72 |710/63 |340/825.52 |235/462.15 |714/25).ccls.	15864

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- EPO Abstracts Database
- JPO Abstracts Database
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- IBM Technical Disclosure Bulletins

Search: L5

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, October 08, 2004 Printable Copy Create Case

Set Name	Query
side by side	
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR
L5	710/3,100,300,305,301,316,1,313,72,63;439/189,497,507,620,505;235/462.15;361/683,686,752,7
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
L4	L3
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR
L3	L1 same (signal near5 pin)
L2	L1 and (signal near5 pin)
L1	(select$4 near3 path) near10 pin

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L3 and L5	5

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search

Recall Text Clear Interrupt

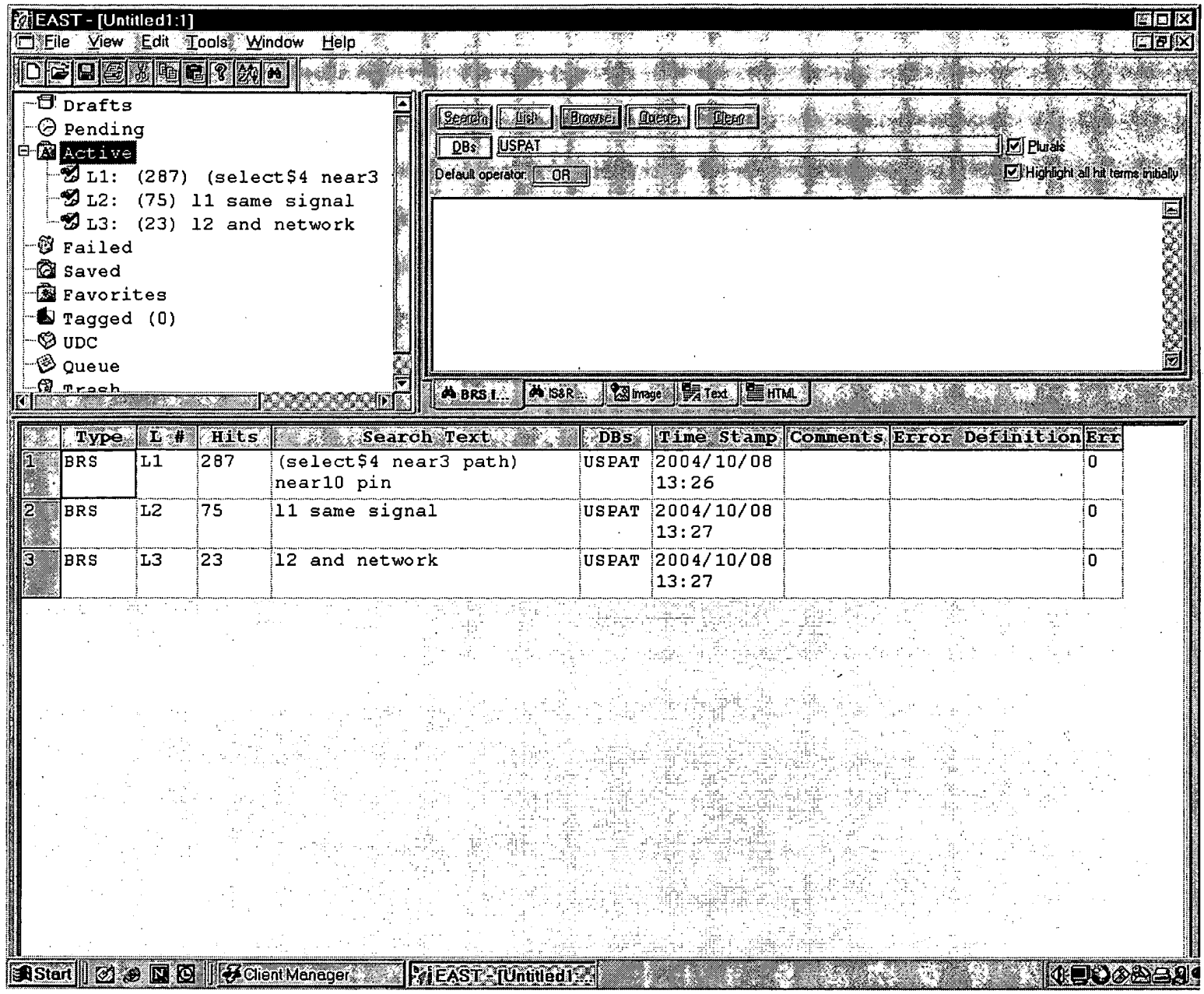
Search History

DATE: Friday, October 08, 2004 Printable Copy Create Case

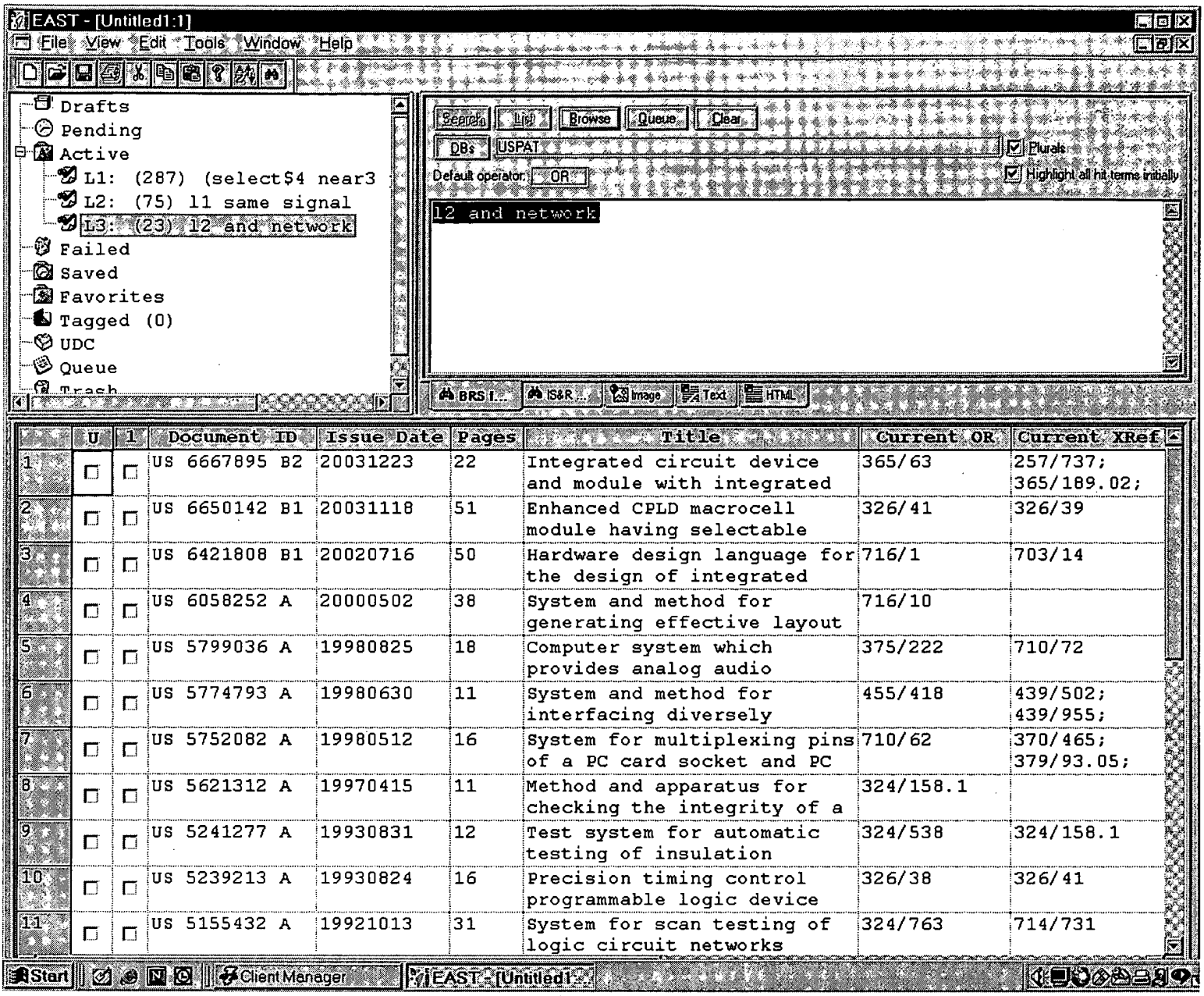
Set Name side by side	Query
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR
L6	l3 and L5
L5	710/3,100,300,305,301,316,1,313,72,63;439/189,497,507,620,505;235/462.15;361/683,686,752,7
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
L4	L3
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR
L3	L1 same (signal near5 pin)
L2	L1 and (signal near5 pin)
L1	(select$4 near3 path) near10 pin

END OF SEARCH HISTORY

h e b b cg b e e ch



	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	287	(select$4 near3 path) near10 pin	USPAT	2004/10/08 13:26			0
2	BRS	L2	75	l1 same signal	USPAT	2004/10/08 13:27			0
3	BRS	L3	23	l2 and network	USPAT	2004/10/08 13:27			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6667895 B2	20031223	22	Integrated circuit device and module with integrated	365/63	257/737; 365/189.02;
2	☐	☐	US 6650142 B1	20031118	51	Enhanced CPLD macrocell module having selectable	326/41	326/39
3	☐	☐	US 6421808 B1	20020716	50	Hardware design language for the design of integrated	716/1	703/14
4	☐	☐	US 6058252 A	20000502	38	System and method for generating effective layout	716/10	
5	☐	☐	US 5799036 A	19980825	18	Computer system which provides analog audio	375/222	710/72
6	☐	☐	US 5774793 A	19980630	11	System and method for interfacing diversely	455/418	439/502; 439/955;
7	☐	☐	US 5752082 A	19980512	16	System for multiplexing pins of a PC card socket and PC	710/62	370/465; 379/93.05;
8	☐	☐	US 5621312 A	19970415	11	Method and apparatus for checking the integrity of a	324/158.1	
9	☐	☐	US 5241277 A	19930831	12	Test system for automatic testing of insulation	324/538	324/158.1
10	☐	☐	US 5239213 A	19930824	16	Precision timing control programmable logic device	326/38	326/41
11	☐	☐	US 5155432 A	19921013	31	System for scan testing of logic circuit networks	324/763	714/731

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select* and path and pin and signal Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Design and VLSI implementation of a novel concurrent 16-bit multip accumulator for DSP applications**
Poornaiah, D.V.; Haribabu, R.; Ahmad, M.O.;
Acoustics, Speech, and Signal Processing, 1993. ICASSP-93., 1993 IEEE International Conference on , Volume: 1 , 27-30 April 1993
Pages:385 - 388 vol.1

[Abstract] [PDF Full-Text (296 KB)] **IEEE CNF**

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2 **Parasitic characteristics of BGA packages**
Chang, T.; Cheng, P.H.; Huang, H.C.; Lee, R.S.; Lo, R.;
IC/Package Design Integration, 1998. Proceedings. 1998 IEEE Symposium on Feb. 1998
Pages:124 - 129

[Abstract] [PDF Full-Text (748 KB)] **IEEE CNF**

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3 **A 2.5 GHz BiCMOS transceiver for wireless LAN**
Meyer, R.G.; Mack, W.D.; Hageraats, J.J.E.M.;
Solid-State Circuits Conference, 1997. Digest of Technical Papers. 44th ISSCC 1997 IEEE International , 6-8 Feb. 1997
Pages:310 - 311, 477

[Abstract] [PDF Full-Text (1172 KB)] **IEEE CNF**

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Design and VLSI implementation of a novel concurr bit multiplier-accumulator for DSP applications

Poornaiah, D.V. Haribabu, R. Ahmad, M.O.
Indian Telephone Ind. Ltd., Bangalore, India;

This paper appears in: **Acoustics, Speech, and Signal Processing, 1993. : 93., 1993 IEEE International Conference on**

Meeting Date: 04/27/1993 - 04/30/1993
Publication Date: 27-30 April 1993
Location: Minneapolis, MN USA
On page(s): 385 - 388 vol.1
Volume: 1
Reference Cited: 20
Inspec Accession Number: 4754281

Abstract:
The authors propose an efficient carry-save algorithm based on the Baugh-W transformation technique and map it onto a novel concurrent multiplier-accun (CMAC) architecture that can be configured on-the-fly for **selecting** multiply multiply-add/subtract computations involving unsigned/**signed** 2's compleme mode data formats. The proposed CMAC does not require the use of a separa module, thereby achieving a reduction of 50% in the computation time along savings in the area when compared with the conventional MACs. The CMAC, w maintaining functional as well as near total **pin** compatibility with the industry MACs, such as the ADSP1010 and TDC 1010 series, provides additional featur mixed-mode data format, saturation arithmetic logic, and on-chip test logic fc measurement of the critical **path** delay. A 16×16 CMAC based on carry-save look-ahead techniques is designed and was extensively simulated with a cycle ms using 1 μm CMOS gate array technology rules

Index Terms:
16 bits Baugh-Wooley transformation CMOS gate array technology CMOS integrate DSP VLSI VLSI implementation area carry logic carry look-ahead techniques c algorithm computation time concurrent multiplier-accumulator critical **path** delay d processing chips logic design mixed-mode data format on-chip test logic **pin** comp saturation arithmetic logic 16 bits Baugh-Wooley transformation CMOS gate array t CMOS integrated circuits DSP VLSI VLSI implementation area carry logic carr

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techniques carry-save algorithm computation time concurrent multiplier-accumulato **path** delay digital **signal** processing chips logic design mixed-mode data format o logic **pin** compatibility saturation arithmetic logic

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Search Results - Record(s) 1 through 5 of 5 returned.

☐ 1. Document ID: US 20040039863 A1

Using default format because multiple data bases are involved.

L6: Entry 1 of 5 File: PGPB Feb 26, 2004

PGPUB-DOCUMENT-NUMBER: 20040039863
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040039863 A1

TITLE: Spare input/output buffer

PUBLICATION-DATE: February 26, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Isom, Melvin T. III	Durham	NC	US	
Hegde, Shailesh U.	Cary	NC	US	

US-CL-CURRENT: 710/305

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 6738858 B1

L6: Entry 2 of 5 File: USPT May 18, 2004

US-PAT-NO: 6738858
DOCUMENT-IDENTIFIER: US 6738858 B1

TITLE: Cross-bar matrix for connecting digital resources to I/O pins of an integrated circuit

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 5799036 A

L6: Entry 3 of 5 File: USPT Aug 25, 1998

US-PAT-NO: 5799036
DOCUMENT-IDENTIFIER: US 5799036 A

TITLE: Computer system which provides analog audio communication between a PC card

h e b b g e e e f e g ef b e

and the computer's sound system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 4. Document ID: US 5752082 A

L6: Entry 4 of 5 File: USPT May 12, 1998

US-PAT-NO: 5752082
DOCUMENT-IDENTIFIER: US 5752082 A

TITLE: System for multiplexing pins of a PC card socket and PC card bus adapter for providing audio communication between PC card and computer sound system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 5. Document ID: US 4300207 A

L6: Entry 5 of 5 File: USPT Nov 10, 1981

US-PAT-NO: 4300207
DOCUMENT-IDENTIFIER: US 4300207 A

TITLE: Multiple matrix switching system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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Terms	Documents
L3 and L5	5

Display Format: - Change Format

Previous Page Next Page Go to Doc#

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US006058252A

United States Patent [19]

Noll et al.

[11] Patent Number: 6,058,252

[45] Date of Patent: May 2, 2000

[54] SYSTEM AND METHOD FOR GENERATING EFFECTIVE LAYOUT CONSTRAINTS FOR A CIRCUIT DESIGN OR THE LIKE

[75] Inventors: Mark D. Noll, Santa Clara, Calif.; Kenneth E. Scott, Sherwood, Oreg.; Robert L. Walker, Boulder, Colo.

[73] Assignee: Synopsys, Inc., Mountain View, Calif.

[21] Appl. No.: 08/910,803

[22] Filed: Aug. 13, 1997

Related U.S. Application Data

[63] Continuation of application No. 08/375,455, Jan. 19, 1995, abandoned.

[51] Int. Cl.[7] G06F 9/455; H01L 21/70

[52] U.S. Cl. 395/500; 364/490; 364/491

[58] Field of Search 364/488, 489, 364/490, 491, 578; 395/500

[56] References Cited

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4,593,363	6/1986	Burstein et al. .	
4,615,011	9/1986	Linsker .	
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5,158,455	12/1992	Hooper .	
5,191,541	2/1993	Landman et al. .	
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5,432,709	9/1995	Dai et al.	364/578
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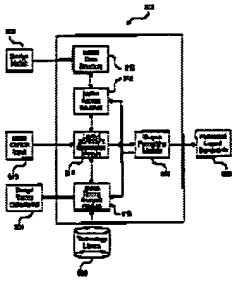
The Olympus Synthesis System, Giovanni De Micheli et al., IEEE, Oct., 1990.

Primary Examiner—Kevin J. Teska
Assistant Examiner—Dan Fiul
Attorney, Agent, or Firm—Kolisch, Hartwell, Dickinson, McCormack & Heuser

[57] ABSTRACT

A computer system and computer implemented method for deriving constraints with which to direct automatic integrated circuit layout is disclosed. The present invention is particularly adapted for use in the design of large integrated circuits with complex synchronous timing behavior. Preferably, the invented computer system includes means for storing a netlist data structure within a storage means is provided, the netlist data structure representing a circuit configuration having a plurality of circuit elements and representing static timing information for the circuit configuration; means for selecting specified circuit elements to be used for generating the layout constraints, whereby the specified circuit elements that are selected are fewer than, i.e. represent a proper subset of, the plurality of circuit elements of the circuit configuration; means for identifying a most critical path through each of the specified circuit elements based upon the static timing information, whereby preferably the most critical path is that path having the least slack defined as the difference between a required time at which a signal should reach the specified circuit element and an arrival time at which the signal is expected to reach the specified circuit element; and means for generating layout constraints from the most critical path through each of the specified circuit elements, whereby at least one constraint is generated covering each of the specified circuit elements. Also disclosed is a feature whereby any paths that do not meet specified filter criteria, and paths that are duplicates of others, are discarded, thereby retaining only fraudulent critical paths on which to base layout constraints.

16 Claims, 17 Drawing Sheets



US005774793A

United States Patent [19]

Cooper et al.

[11] Patent Number: 5,774,793

[45] Date of Patent: Jun. 30, 1998

[54] **SYSTEM AND METHOD FOR INTERFACING DIVERSELY CONTROLLED DEVICES TO A BUS CONNECTOR HAVING A COMMON SIGNAL FORMAT**

[75] Inventors: Gershon N. Cooper, Encino; Andrew Holman, West Hills, both of Calif.

[73] Assignee: ORA Electronics, Inc., Chatsworth, Calif.

[21] Appl. No.: 361,985

[22] Filed: Dec. 22, 1994

[51] Int. Cl.[6] H04B 1/38

[52] U.S. Cl. 455/89; 455/345; 455/127; 379/59; 439/502; 439/955

[58] Field of Search 455/89, 90, 127, 455/128, 344, 345, 346, 347, 348, 349, 350, 351, 33.1; 379/58, 59, 63, 441, 442; 439/502, 636, 505, 955

[56] References Cited

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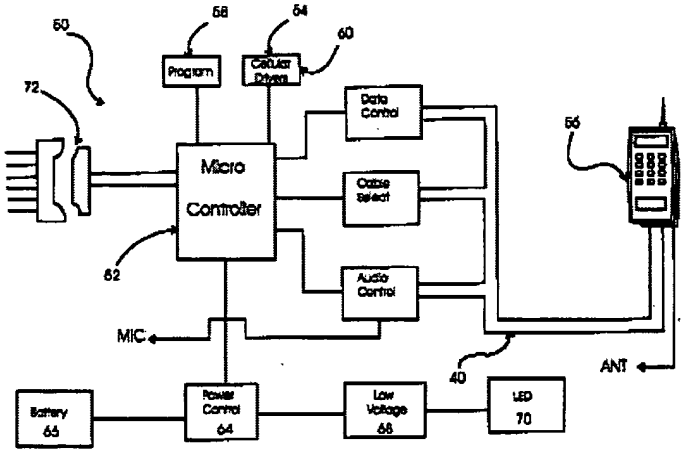
5,479,479	12/1995	Braitberg et al.	379/59

Primary Examiner—Reinhard J. Eisenzopf
Assistant Examiner—Dwayne D. To
Attorney, Agent, or Firm—Matthew P. Jodziewicz

[57] **ABSTRACT**

A system for connecting a plurality of cellular telephones, each responsive to device-specific command signals for its operation, to an automotive electronics and communications system through a bus connector having a known universal signal format, includes a docking station having a cradle member shaped for receiving at least one cellular telephone. An interface unit contains the hardware and firmware drivers necessary for controlling the selected cellular telephone. A user selected cable having a specific signal path configuration selects the needed drivers. A second cable connects the interface unit with the bus connector for communicating signals therebetween.

42 Claims, 4 Drawing Sheets



United States Patent [19]
Whetsel

[11] **Patent Number: 5,056,093**
[45] **Date of Patent: Oct. 8, 1991**

[54] **SYSTEM SCAN PATH ARCHITECTURE**

[75] Inventor: Lee D. Whetsel, Plano, Tex.
[73] Assignee: Texas Instruments Incorporated, Dallas, Tex.

[21] Appl. No.: 391,781
[22] Filed: Aug. 9, 1989
[51] Int. Cl.[5] G01R 31/28
[52] U.S. Cl. 371/22.3; 371/22.1
[58] Field of Search 371/22.3, 22.1; 324/73.1

[56] **References Cited**
U.S. PATENT DOCUMENTS

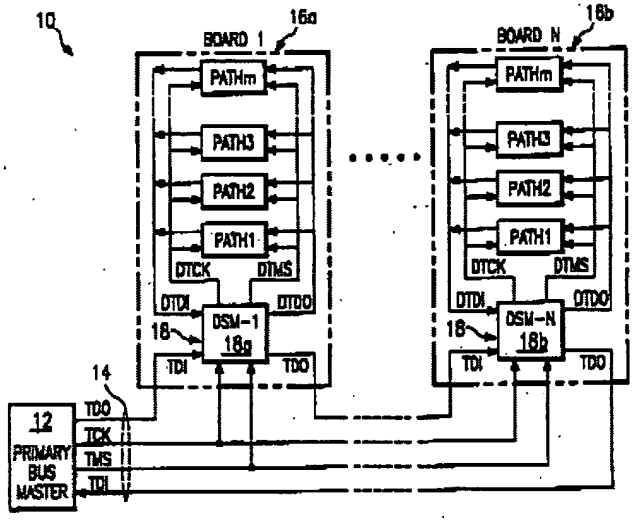
4,494,066 1/1985 Cosi et al. 371/22.3
4,710,931 12/1987 Bailey et al. 371/22.3
4,872,169 10/1989 Whetsel 371/22.3

Primary Examiner—Charles E. Atkinson
Attorney, Agent, or Firm—B. Peter Barndt; James T. Comfort; Melvin Sharp

[57] **ABSTRACT**

A system scan path architecture is provided by a device select module (DSM) (18) which may be used in conjunction with associated circuits (16a-b) to select secondary scan paths (PATH1-m) on each circuit for coupling with a primary scan path on a test bus (14). The test bus (14) is controlled by a primary bus master (12). Remote bus masters (12a) may be used in conjunction with the DSMs (18) to provide serial-scan testing independent of the primary bus master (12).

41 Claims, 11 Drawing Sheets



United States Patent [19]
Jackson

[11] **3,922,537**
[45] **Nov. 25, 1975**

[54] **MULTIPLEX DEVICE FOR AUTOMATIC TEST EQUIPMENT**

[75] Inventor: Philip C. Jackson, Mahwah, N.J.

[73] Assignee: Instrumentation Engineering, Inc., Franklin Lakes, N.J.

[22] Filed: Sept. 26, 1974

[21] Appl. No.: 509,592

[52] U.S. Cl. ..... 235/153 AC; 324/73 R
[51] Int. Cl.² G01R 31/28
[58] Field of Search ..... 235/153 AC; 324/73 R, 324/73 AT; 340/172.5

[56] **References Cited**
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B-H Research Laboratories, Inc., 4500/4600 Series Automated Test Systems, pp. 11–17.

Primary Examiner—R. Stephen Dildine, Jr.
Attorney, Agent, or Firm—Morgan, Finnegan, Pine, Foley & Lee

[57] **ABSTRACT**

The present invention pertains to multiplex apparatus for an automatic computerized diagnostic testing system for selectively interconnecting peripheral measurement and stimulus devices to a unit under test (UUT) through various switching subsystems which differ in switching capability, load carrying ability, frequency bandwidth, and mode of operation. The multiplexer includes plural conducting means between each pin of the circuit under test and corresponding terminals or test points of plural switching sub-systems used to interconnect UUT pins and the peripheral testing devices. Each plural conducting means includes controllable switch means. These switch means operate automatically under programmed computer control. One of the switching subsystems has high frequency signal carrying ability, and the conducting means associated with this subsystem preferably include impedance matching buffers, and have a frequency bandwidth equal to that of the subsystem.

13 Claims, 7 Drawing Figures